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# Ultrathin flexible planar crystalline-silicon/polymer hybrid solar cell with 5.68% efficiency by effective passivation

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ABSTRACT

Ultrathin silicon based solar cells provide a viable way to reduce the material usage and diversify their applications. However, complex light-trapping structures are always needed to be fabricated to enhance light absorption, which will lead to exacerbation of carrier collection and expensive fabrication cost. Here, we report very simple planar flexible crystalline silicon-polymer hybrid solar cell with thickness about 18 μm, whose power conversion efficiency (PCE) reaches 5.68%. By introducing the amorphous silicon layer to passivate the Silicon/Polymer interface in our device, with accuracy control of the thickness of 2 nm to balance the passivation effect and the deterioration of internal electric field, the short current density reaches 83.0% of the theoretical limit. Additionally, we found that the average PCE of solar cells passivated by such technology is 5.8% and 7.1% enhanced compared with those without passivation (H-terminated) and passivated by native oxide approaches. The simple device structure provided in this study has great practicability, and the passivation processes can be duplicated for other silicon based photovoltaic devices.



## 1. Introduction

Ultrathin solar cells provide an effective way of reducing material usage, utilizing low quality material and realizing diverse like flexible applications [1–3]. Along with fabrication techniques for ultrathin crystalline silicon (c-Si) wafer that have advanced to a level where desired thickness, roughness and composition can be readily synthesized by etching and other techniques [4–6], ultrathin c-Si based solar cells especially the c-Si/polymer hybrid ones have attracted a lot of attention [7–12]. This is because such c-Si/polymer solar cell is much suitable to realize low temperature and large area fabrication as it does not require a complex junction fabrication process and it usually has simple structures [13,14].

It has been reported that the power conversion efficiency (PCE) of ultrathin c-Si/PEDOT:PSS device has reached 6.6% [13]. Where Sharma et al have made great efforts in fabricating light-trapping structures, including silicon pillars on the front-surface and silver particles on the back-surface, to enhance light absorption. Indeed, the photocurrent density of devices having these structures is dramatically enhanced. However, these complex architectures have also brought about abundant energy losses (carrier recombination) due to the increased interface defects. Such increased energy losses can be reflected by the fact that, the ratio of the measured photocurrent density to the theoretical limit (R-M/T) for device with light-trapping architectures (51%, 18.50 to 36.51 mA $cm^2$) is much lower than that of device without light-trapping architectures (76%, 15.06 to 19.94 mA $cm^2$) [13]. Additionally, the light-trapping structures also complicate the fabrication process thus increasing the cost, and as a result it is difficult to ensure the process consistency. From the above considerations, planar ultrathin solar cells are more suitable for practical application.

In this work, we fabricate simple planar c-Si/PEDOT:PSS solar cell of about 18 μm thickness, which has good flexibility. Focusing on reducing the carrier recombination, two passivation technologies have been carried out. The two passivation technologies are native oxidizing and depositing intrinsic amorphous silicon (i a-Si) on the silicon at the c-Si/PEDOT:PSS interface. The depositing of i-a-Si layer is the best method, and by controlling its thickness to 2 nm the PCE of device can reach 5.68% with R-M/T about 83.0%.

## 2. Experiments

### 2.1. Fabrication of ultrathin silicon

originally, the n-type (1 0 0), double side-polished, 4-in. silicon wafers (resistivity, 1–5 Ω cm) with a thickness of 500 ± 10 μm were

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ultrasonically cleaned in acetone, ethanol and deionized water for 10 min, respectively. Subsequently, the substrates were rinsed with deionized (DI) water and dried with a nitrogen gun. After that, the clean silicon wafers were immersed in KOH solution with concentration of 50 wt.% at 90 °C for certain duration of time, to obtain 18 μm free-standing c-Si membranes.

### 2.2. Silicon passivation

the ultrathin c-Si wafer is first cleaned by deionized (DI) water. The samples without passivation were treated by immersing the silicon wafer into HF solution (V:V = 1:2) at room temperature for 2 min; the native oxide method was done by placing the HF-cleaned wafer in a dry dish with air condition; and the amorphous silicon passivation was carried out by depositing i a-Si layer on the HF-cleaned silicon wafer using the PECVD equipment for 20s at 250 °C. In the i a-Si deposition process, a 165 sccm mixture gas flow of $SiH_4$/Ar (1/24) was used; and the chamber pressure maintained about 3 Pa.

### 2.3. Fabrication of photovoltaic devices

firstly, the ultrathin c-Si of thickness 18 μm was cut into small squares of 1 × 1 $cm^2$. Then, small silicon squares without passivation (H-terminated), with native oxide layer or i a-Si layer were prepared; highly conductive PEDOT:PSS solvent was prepared by mixed the PEDOT:PSS (purchased from Bayer AG) with dimethyl sulfoxide (DMSO, 5 wt%) and Zonyl fluoro-surfactant (0.1 wt%). Thereafter, these silicon squares were transferred into the $N_2$-filled glove box and PEDOT:PSS was spin-coated on their front surface at 3000 rpm for 60 s, followed by hot plate baking at 150 °C for 15 min. After this, we deposited a continuous thin film of 150 nm Ag as a bottom electrode and a finger-grid of 100 nm Ag as a top electrode. The width of each finger was 80 μm, and the spacing between fingers was 920 μm.

### 2.4. Characterization

morphologies of the silicon samples were characterized using scanning electron microscopy (SEM; Hitachi S-5500). The passivation layers of the native oxidation and i a-Si were characterized by the transmission electron microscopy (TEM, Libra 200FE) at 200 kV. The cross-sectional TEM samples were prepared through a conventional mechanical polishing process including cutting, grinding, polishing, and a final ion-milling thinning step. The minority carrier lifetimes were characterized by a microwave photo-conductance decay (μ-PCD) technique (WT2000PVN, Semilab). The current-voltage characteristics of the solar cells are measured using Keithley 2400 under 100mW/$cm^2$ illumination.

## 3. Results and discussions

### 3.1. Flexibility and device structure of the ultrathin planar hybrid solar cell

The SEM image of ultrathin silicon with thickness about 18 μm (used in fabricating solar cells) is given in Fig. 1(a). Through illuminating with white light, as shown in Fig. 1(b), it can be intuitively observed that such ultrathin silicon can absorb most of the light with wavelength smaller than 700 nm (red light).

By several tests we found that the silicon wafer with such thickness has excellent mechanism flexibility. For example, it could be bent into a ring, Fig. 1(c), be warped, Fig. 1(d) and be cut like a piece of paper, Fig. 1(e). Such flexible features of the ultrathin silicon indicate that the photovoltaic devices based on ultrathin silicon may also possess good flexibility thus have diverse applications. The inset in Fig. 1(g) shows that a c-Si/PEDOT:PSS solar cell sample we fabricated stuck on the copper foil tape, which is bent on a glass rod of diameter 6 mm.

The solar cells fabricated in this study own very simple planar structure, as shown in Fig. 1(f). As mentioned in the experiment section, it can be fabricated by a simple spin-coated process. However, this device structure contains an inorganic/organic interface which will bring in abundant carrier recombination. So, effective passivation should be a key technology to limit carrier recombination and increasing the photocurrent and efficiency of silicon/polymer hybrid solar cells [15–21]. Therefore, in this study we introduce a passivation layer at the interface between the silicon and the PEDOT:PSS layer, and different passivation methods were tested. By using the best passivation approach, inserting the i a-Si layer at the interface, a PCE of 5.68% has been achieved, as shown in Fig. 1(g).

### 3.2. Passivation effects by two different technologies

To reduce carrier recombination at the Si/PEDOT:PSS interface, two passivation technologies have been used in this study. The first one is the native oxidizing method, which has been widely used in silicon-based hybrid solar cells [22,23]; and the second one is to

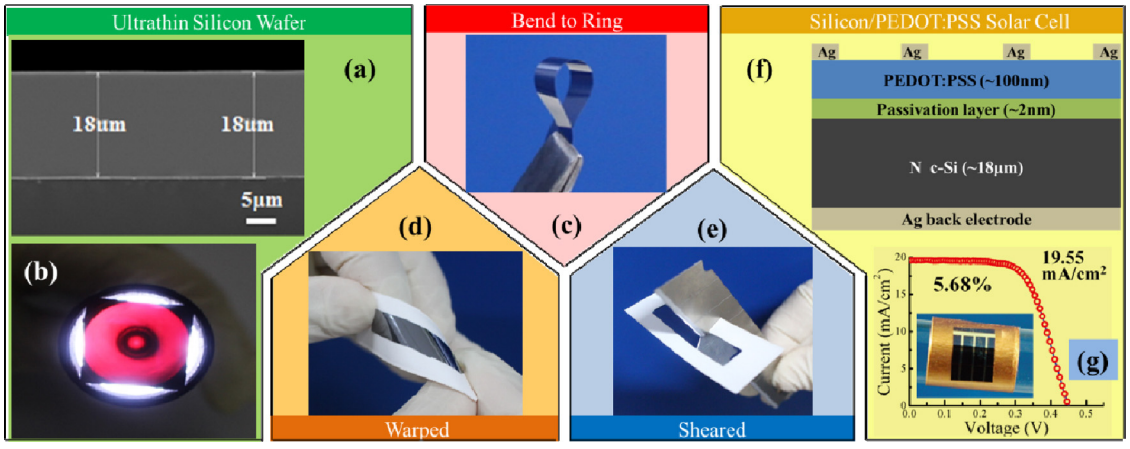


**Fig. 1.** (a) SEM images of our fabricated ultrathin silicon wafer; (b) Optical image of the ultrathin silicon illuminated by white light; (c) Ultrathin silicon ring bent by a tweezer; (d) Kinking of the ultrathin silicon, stuck on white paper. (e) Ultrathin silicon stuck on white paper can be cut just like a piece of paper. (f) Schematic illustration of the solar cell structure. (g) Current–voltage curve of the solar cell with efficiency 5.68% and short current density 19.55 mA/$cm^2$, where the inset illustrates the flexibility of device, by sticking it on a copper foil tape, which is bent on a glass rod of diameter 6 mm.

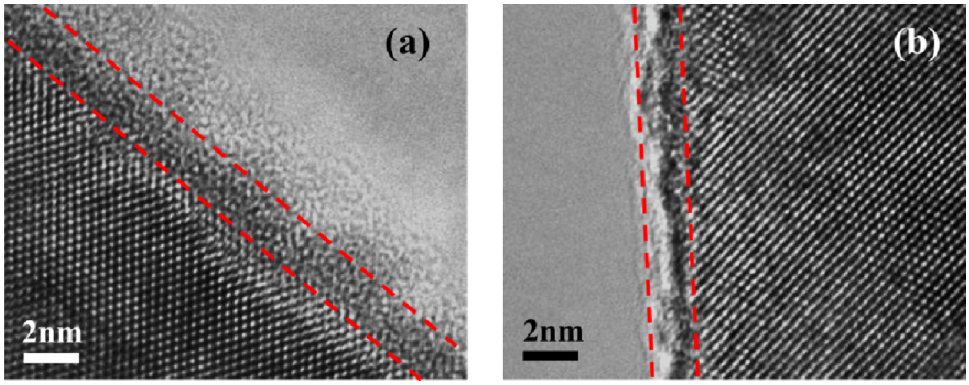


**Fig. 2.** TEM images of silicon surface (a) deposited by i a-Si layer and (b) after native oxidation.

deposit an i a-Si layer on the silicon surface, which is referred from the passivation technology in solar cells [24–27]. Comparisons have been carried out for the passivation effects between the samples passivated by these two methods and the ones without passivation (H-terminated). For the samples passivated by these two methods, a silica or i a-Si insert layer was introduced between the silicon and the PEDOT:PSS, respectively. This intercalation acts as a barrier, so its thickness has great influence on the internal electric field thus exerting influence on carrier separation according to the quantum tunneling theory. Therefore, it is of great necessity to control the thickness of the silica or i a-Si intercalation. After a great deal of tests (given in the supporting information), we find that the optimal process for the native oxidation method is to treat the silicon wafer for 12 h at room temperature in air condition; and the optimal process for the i a-Si passivation method is to deposit the intrinsic amorphous silicon at 250 °C for 20 s. What's shown in Fig. 2 are the TEM images of the silicon surface passivated by an i a-si layer and silica layer, corresponding to the optimized process. It can be found that the passivation layers had apparent boundaries with the c-Si substrate. The thickness of the optimal i a-si layer is about 2 nm, while that of the silica layer is about 1.5 nm.

To characterize the passivation effects, we measured the minority carrier lifetimes of the silicon wafers treated by above two technologies, as shown in Fig. 3. From which we can see that the i a-Si passivation is the best method. The minority carrier lifetime of the silicon wafer passivated by an i a-Si, about 41.35 μs,

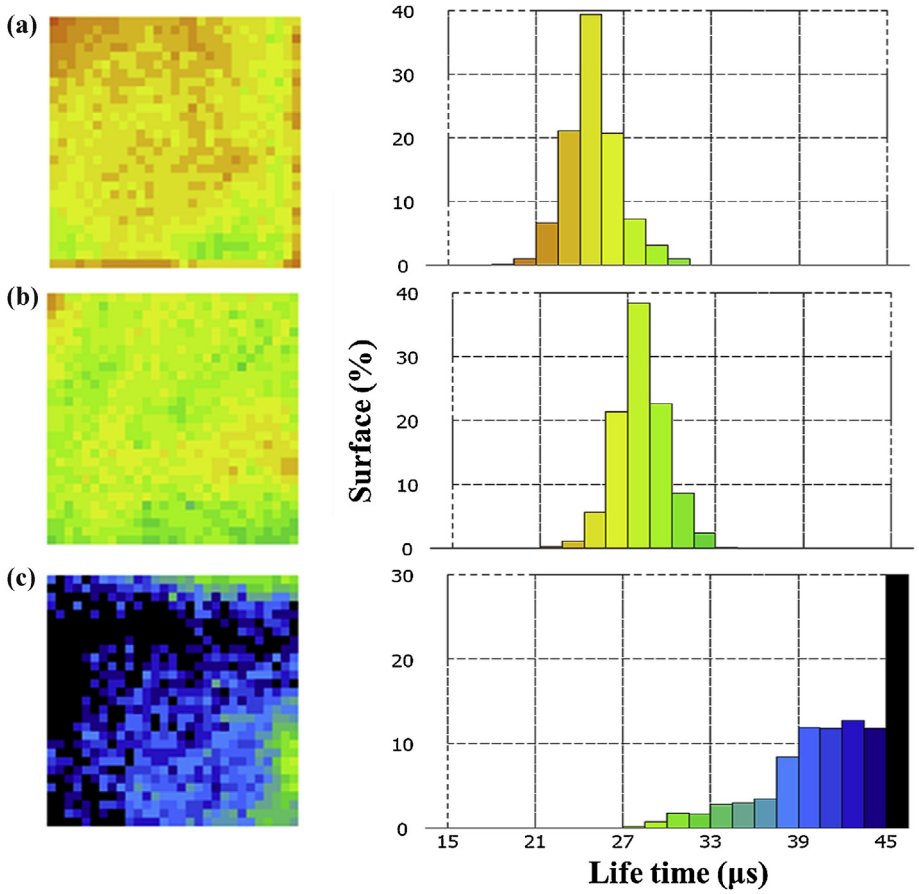


**Fig. 3.** Spatial mapping of the minority carrier lifetimes for samples by different passivation methods. (a) Native oxide, (b) HF-treated, and (c) i a-Si passivation. The area of the silicon wafers are $15 \times 15\,mm^2$.

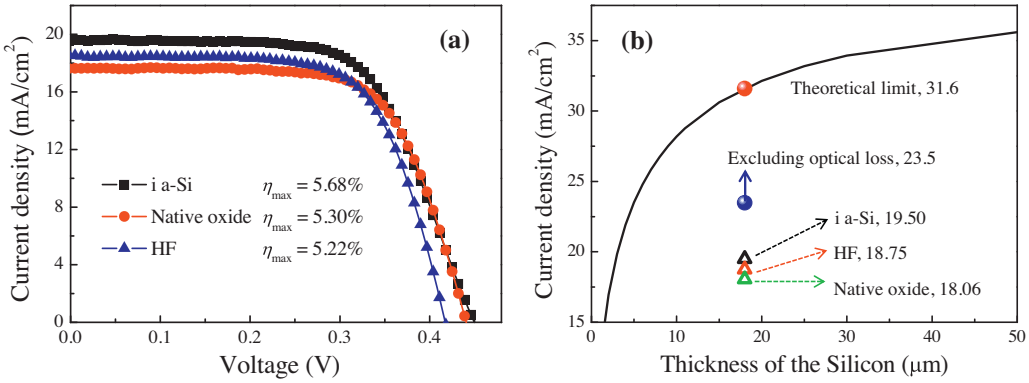


**Fig. 4.** (a) Current density–voltage characteristics of the Si/PEDOT:PSS heterojunction solar cells using different passivation technologies. (b) Comparisons between the average current density for solar cells passivated by different methods and the theoretical limit excluding the optical loss (reflectance and transmission).

is much higher than those of the H-terminated silicon surface and passivated by a native oxidation layer, 27.88 μs and 24.70 μs respectively. It is worth mentioning that the samples without passivation (H-terminated) and that passivated by native oxidation also perform well, since the minority carrier lifetimes of such samples are higher than that (21.10 μs) treated by the optimal wetting oxidation technology [23].

The minority carrier lifetime is determined by the surface and bulk recombination [28], as given in Eq. (1) bellow;

$$\frac{1}{\tau_m} = \frac{1}{\tau_b} + \frac{2S}{d} \quad (1)$$

where $\tau_m$ and $\tau_b$ is the measured lifetime and the bulk lifetime respectively, $S$ is the surface recombination velocity, and $d$ is the wafer thickness.

To characterize the surface passivation effect, eliminating the influence from thickness, we have also calculated the $S$ values from Eq. (1). In our calculations, $\tau_b$ = 19 ms is used [28], and the wafer thicknesses are all assumed to be 500 μm. The $S$ values obtained are 1051, 895 and 603 cm/s, for the native oxidized, H-terminated, and i a-Si passivated silicon surfaces, respectively. These results also demonstrate that the i a-Si passivation method is the best, which is consistent with the device performances as given below.

### 3.3. Device performance

The current-voltage characteristics of the planar ultrathin c-Si/PEDOT:PSS solar cells using above passivation technologies are shown in Fig. 4(a). Apparently, the device using the i a-Si passivation method possesses the highest short current density $J_{sc}$ and open voltage $V_{oc}$, thus the best performance (PCE = 5.68%).

The average values of $J_{sc}$ and $V_{oc}$ including standard deviation from several solar cell devices are listed in Table 1. Firstly, it can be seen that the $V_{oc}$ of devices passivated by i a-Si is 6.6% and 8.4% higher than those without passivation and passivated by native oxidation, respectively. This improvement can be mainly attributed to the atomic scale rough surface of the deposited i a-Si layer, which is better for the formation of high quality hetero junction between the c-Si and the PEDOT:PSS layer. Then, the $J_{sc}$ of solar cells passivated by the i a-si is also enhanced by 4.0% and 8.0%, compared with those without passivation and passivated by native oxidation layer. The increased $J_{sc}$ can be directly related to better passivation of the i a-Si layer.

**Table 1**
Photovoltaic characteristics of Si/PEDOT:PSS solar cells with different passivation.

| Passivation | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | $FF$ (%) | $\eta$ (%) |
|---|---|---|---|---|
| i a-Si | 438 ± 7 | 19.50 ± 0.22 | 62.12 ± 2.28 | 5.30 ± 0.21 |
| H-terminated | 411 ± 7 | 18.75 ± 0.17 | 64.97 ± 2.88 | 5.01 ± 0.22 |
| Native oxide | 404 ± 35 | 18.06 ± 0.44 | 64.35 ± 4.15 | 4.71 ± 0.59 |

The passivation effect of different methods can be reflected by the R-M/T of the photovoltaic devices. The limited current density is calculated by integrating the incident solar photon flux density from AM1.5 spectrum in the waveband 300–1100 nm, under the assumption that the internal quantum efficiency is 100%. The obtained results for photovoltaic devices of different thickness are plotted in Fig. 4(b). For the device of 18 μm thickness, we have also calculated the more practical limited current density that excludes optical losses, which means the part of light being reflected (supporting information). The obtained current density is 23.5 mA/cm$^2$. Referring to this value, the R-M/T for devices passivated using the i a-Si, HF treatment and native oxidation methods are 83.0%, 79.8% and 76.9%, respectively. The higher value for the device passivated by an i a-Si layer denotes that this method is an ideal passivation method for c-Si/PEDOT:PSS solar cells. Besides, all the R-M/T values for the devices in this study are dramatically higher than those for the devices with complex light-trapping designs, 51.0% [13]. This demonstrates the remarkable superiority of planar structural ultrathin solar cells.

## 4. Conclusions

In this study, simple planar c-Si/PEDOT:PSS hybrid solar cells of about 18 μm thickness are fabricated, which have good flexibility. The i a-Si and native oxidation passivation technologies are applied to reduce the charge recombination at the inorganic/organic interface. Among them, the i a-Si passivation method shows dramatic advantages compared with the other ones. By controlling the thickness of the i a-Si layer to 2 nm to balance the passivation effect and the deterioration of internal electric field, the short current density of photovoltaic devices can reach 83.0% of the theoretical limit, and the PCE of the simple planar ultrathin flexible c-Si/PEDOT:PSS solar cell can reach 5.68%. This study provides a prospective passivation method for c-Si/PEDOT:PSS solar cells, and a very practical device structure.

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## Appendix A. Supplementary data

Supplementary data associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.apsusc.2016.01.129.

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