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A one-step template-free approach to achieve tapered silicon nanowire arrays with controllable filling ratios for solar cell applications

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A facile and low-cost one-step template-free approach is presented for the fabrication of tapered silicon nanowire (SiNW) arrays. A silver network catalyst is used to chemically etch silicon in a HF/H_2O_2 solution, where the solution is chosen to selectively dissolve the silver network during the etching process, resulting in the formation of tapered SiNWs. Notably, the filling ratio of the tapered SiNWs can be tuned simply by varying the pattern of the silver network. Surface reflection was strongly suppressed in the tapered SiNW arrays (only 400 nm in thickness), which were employed in SiNWs/poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) heterojunction solar cells exhibiting a power conversion efficiency of 6.7%. The tapered SiNW arrays prepared by this one-step template-free method are expected to be efficient structures for a variety of photovoltaic devices.

Introduction

Silicon nanowire (SiNW) arrays have attracted significant interest due to their antireflective and light-trapping properties, which are of great importance for high-efficiency solar cells.[1–3] In particular, SiNW arrays with a tapered structure can suppress reflection over a broad range of wavelengths and angles of incidence through a gradual reduction of the effective refractive index between air and silicon.[4,5] Therefore, scalable procedures for producing tapered SiNW arrays and the study of their influence on device performance, are urgently required for the development of next generation high-efficiency solar cells.

A few methods for the fabrication of tapered SiNW arrays have been proposed to date. These include vapor–liquid–solid growth[6–9] and dry etching[4,10–14] techniques. However, these two vacuum-based approaches require expensive equipment, which limits their scalability and throughput. Recently a two-step wet etching processes to produce tapered SiNW arrays has been reported.[15,16] SiNWs are formed by metal-assisted chemical etching, where silver nanoparticles applied from solution are used as the catalyst. The SiNWs are then immersed in a KOH solution to produce a tapered structure, where the tapering was reported to result from anisotropic silicon etch rates.[15] Although the wet etching approach reduces the fabrication cost, the need for two etching processes introduces complexity. Furthermore, the control of the structural characteristics, particularly the filling ratio of the tapered SiNWs, is difficult to be realized using this process. Therefore, the development of a facile and low-cost fabrication approach for tapered SiNW arrays with tunable filling ratio is necessary.

In this work, a one-step template-free method is presented for the fabrication of tapered SiNW arrays with various filling ratios. A silver network catalyst is deposited onto the silicon surface using a simple sputter coater and tapered SiNW arrays are obtained through a one-step chemical etch in HF/H_2O_2 solution. By varying the sputtering conditions we control the initial surface coverage and hence the SiNW density. By careful selection of the etching solution we induce *in situ* oxidative dissolution of the silver network and the formation of tapered SiNWs. We demonstrate the ability to reduce surface reflection from silicon by introducing the tapered SiNW arrays and by controlling their density, and likewise demonstrate the ability to improve the performance of a SiNW/poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) heterojunction solar cell by controlling these parameters.

Experiments

In our experiments, n-type Si(100) wafers with a resistivity of 3–5 Ω cm were used and cleaned following previously reported procedures.[17] The silver network was deposited on the cleaned silicon surface by magnetron sputtering with a Quorum Q150-TS sputter coater. Silicon samples covered by the silver network

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were then immediately immersed into the etching solution containing 5 M HF and 0.2 M H_2O_2. The etching process was performed for 10–120 s at room temperature. After etching, silicon samples were immersed into a concentrated HNO_3 cleaning solution to remove any remaining silver and then placed into 7.3 M HF to remove the oxide layer.

In order to verify the performance of the tapered SiNWs, we fabricated prototype SiNW/PEDOT:PSS solar cells similar to those previously reported.[18,19] A 150 nm thick silver layer was deposited by magnetron sputtering onto the backside of the Si substrate to form the rear contact. Highly conductive PEDOT:PSS solution was prepared by mixing commercial PEDOT:PSS (Clevios PH1000) and 5 wt% dimethyl sulfoxide (DMSO). A two thirds volume ratio of isopropyl alcohol was then added into the PEDOT:PSS solution to get good wettability. The PEDOT:PSS solution was spin coated onto the tapered SiNW arrays at 1000 rpm for 60 s and then annealed at 140 °C for 10 min on a hot plate in atmosphere to form SiNWs/PEDOT:PSS heterojunctions. Finally, a silver grid was deposited on the top of the PEDOT:PSS by magnetron sputtering with a shadow mask.

The morphological characteristics of the tapered SiNWs were observed by scanning electron microscopy (SEM) with a FEI Quanta 200F and by high resolution transmission electron microscopy (HRTEM) with a Tecnai G^2 F20. The total reflection spectra were measured using a solar cell IPCE/QE measurement system with an integrating sphere. The current density *versus* voltage (*J–V*) characteristics of the solar cells were recorded using a Keithley 2400 sourcemeter under a solar simulator (XES-301S+EL-100 class AAA) at AM 1.5 condition.

Results and discussion

Fig. 1 shows the morphological characteristics of the tapered SiNWs obtained using our sputtered silver network catalyst and one-step wet etching method (120 s etch). The ordered and vertical alignment of the SiNWs on the silicon substrate is observed in the 45° tilted SEM image (Fig. 1(a)). The length of the SiNWs is in the range of 240–460 nm. Notably the nanowires have the desired tapered shape along the nanowire axial direction from the tip to the root, which is clearly observed in the TEM image of an individual nanowire (Fig. 1(b)). The tapering degree of the nanowire is about 12.7°. Moreover, the HRTEM image in Fig. 1(c) displays that the nanowire has smooth sidewalls and even retains the single-crystal characteristic of the original silicon wafer, as is also revealed by the selected area electron diffraction pattern in the inset image of Fig. 1(c). These results indicate that the one-step chemical etching of silicon is a facile fabrication method for tapered SiNW arrays.

The morphology of the tapered SiNW arrays in the present work is closely associated with that of the silver network catalyst. In the metal-assisted chemical etching process, silver particles serve as the catalysts to facilitate the generation of silicon oxide at the silver/silicon interface, then the silicon oxide is subsequently dissolved by the HF solution, leading to selective etching of the silicon.[20] To get vertical arrays of isolated SiNWs, a high density of silver particles is therefore essential. High-density silver nanoparticle networks, such as those produced in this work, have a collective interaction[21,22] that limits the movement of single particles into the bulk silicon in random downward directions. As a result, dense particles sink along the vertical direction, producing vertical array of SiNWs. If the standard reduction potential of oxidizing agents in the solution is greater than that of silver, silver particles can be oxidized to silver ions, causing a variation in the size and morphology of particles during their sinking process.[23–25] In view of these points, we designed our silver catalyst and etching solution accordingly. The network-like configuration of silver enhances the collective interaction between catalysts, which promotes generation of vertical arrays of SiNWs. Meanwhile, the introduction of a suitable concentration H_2O_2 into the HF solution resulted in a gradual oxidation and shrinkage of the silver network during its sinking process. These synergetic effects resulted in the formation of tapered SiNW arrays.

To confirm the above analysis, morphological evolution of the silver network during etching was investigated. The morphology of the as-deposited silver network is shown in Fig. 2(a). After etching the silicon sample in HF/H_2O_2 solution for 10 s, the original network was split into isolated nanoislands of a similar size, as shown in Fig. 2(b). When the etching duration was increased to 30 s, SiNW arrays were observed on the silicon substrate (Fig. 2(c)). From the inset in Fig. 2(c), it can be clearly seen that these silver nanoislands sink into the bulk silicon. Moreover, the size of silver nanoislands slightly decreased in comparison to that in Fig. 2(b). These results clearly indicate that the tapered nanowire structure follows from the *in situ* oxidation of the silver catalyst and that the

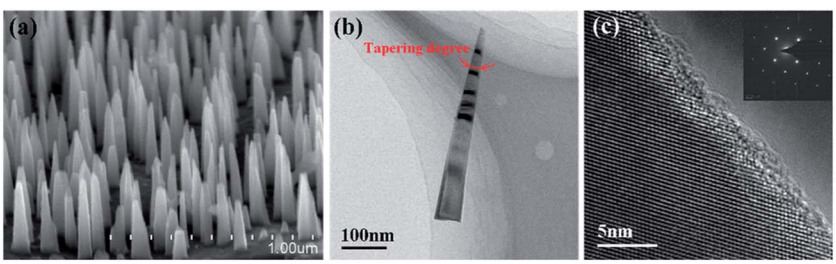


Fig. 1 (a) SEM image (45° tilt) of tapered SiNW arrays; (b) TEM image and (c) HRTEM image of an individual nanowire. Inset image is the pattern of selected area electron diffraction corresponding to (c).

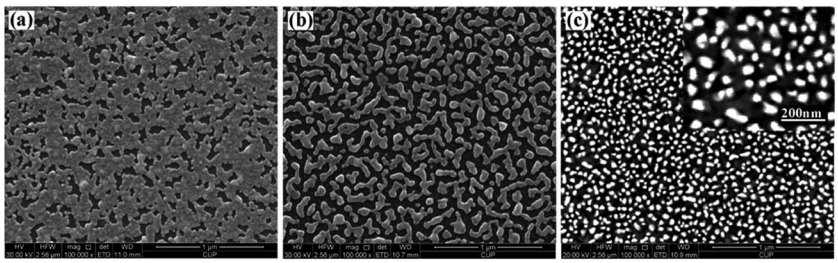


Fig. 2 Planar-view SEM images of the silver network catalyst on a silicon substrate for different etching durations. (a) 0 s; (b) 10 s; (c) 30 s.

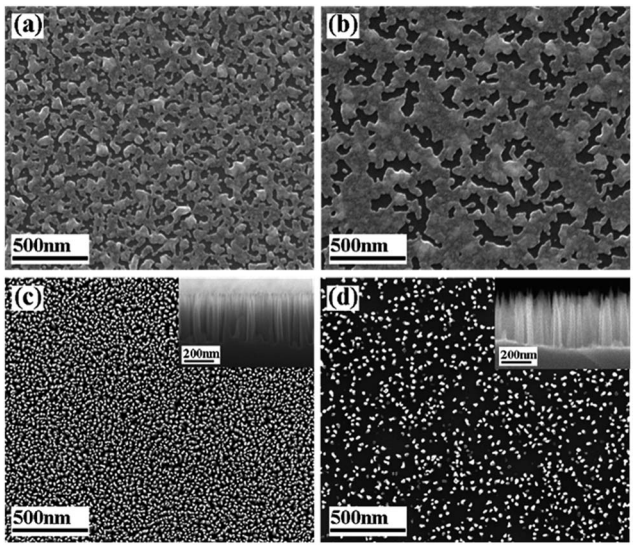


Fig. 3 SEM images of silver network catalysts obtained by different sputtering times and currents. (a) 50 s/10 mA; (b) 55 s/15 mA. SEM images of (c) dense and (d) sparse tapered SiNW arrays obtained by 2 min etching of catalysts in (a) and (b) respectively. Inset images show the cross-sectional morphology corresponding to dense and sparse SiNW arrays.

morphology of the tapered SiNWs is strongly dependant on the original pattern of the silver network.

Based on the above analysis, control over the filling ratio of the tapered SiNWs was realized by varying the original pattern of the silver network. The network in Fig. 3(a) is characterized by small particles and a high density of pores. On the contrary, in Fig. 3(b) the particle clusters are large and the voids more sparse. These different silver network catalyst configurations were achieved by varying sputtering times and sputtering currents precisely. Following the one-step chemical etching of these samples, dense and sparse tapered SiNW arrays were obtained, and their morphologies are shown in Fig. 3(c) and (d), respectively. The filling ratio of the dense and sparse SiNWs is about 5.48×10^8 mm^{-2} and 1.57×10^8 mm^{-2}, respectively. From the insets in Fig. 3(c) and (d), it can be seen that the dense and sparse SiNW arrays have an approximate thickness of 400 nm. It is worth emphasizing that the control of the filling ratio demonstrated here for the tapered SiNWs doesn't require conventional templates or complicated lithography, yet it permits tailoring of the optical properties of the SiNW for application in a variety of solar cells.

The total reflection spectra of the dense and sparse tapered SiNWs were measured and are shown in Fig. 4. Compared to the polished silicon wafer, sparse SiNWs with a length of 400 nm reduce the average reflectance from 39.6% to 10.5% in the wavelength range of 300–1000 nm. The reflection is further suppressed by increasing the filling ratio of the tapered SiNWs. The average reflectance of the dense SiNWs is about 1.6%, which is 6 times lower than that of the sparse SiNWs and similar to the lowest values previously reported for tapered SiNWs made by other techniques.[12,14,16] The difference in antireflective properties between the dense and sparse SiNWs is attributed to different effective refractive index (RI) mismatches at the air/Si interface[15] and to enhanced multiple scattering effects in the dense SiNWs.[5]

To demonstrate their applicability to solar cells, tapered SiNWs were used to construct Si/PEDOT:PSS heterojunctions, as shown schematically in Fig. 5(a). In these devices, light is absorbed by the tapered SiNWs, the photogenerated holes move toward the PEDOT:PSS, and the photogenerated electrons move along the SiNWs toward the back electrode.[26] For comparison, a planar Si/PEDOT:PSS solar cells with similar structure was fabricated as well. Fig. 5(b) shows the typical current density–voltage characteristic of the tapered SiNWs/PEDOT:PSS heterojunction solar cells and the planar Si/PEDOT:PSS solar cells under 1 sun illumination (AM 1.5). The corresponding

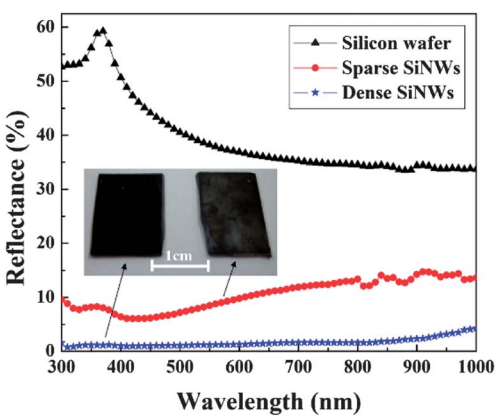
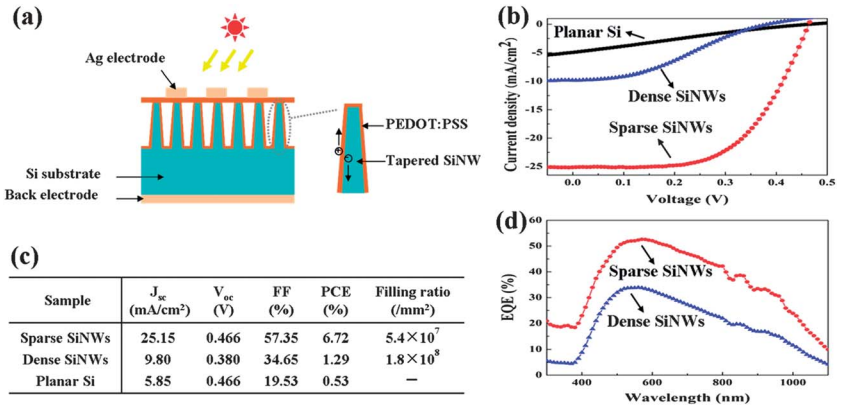


Fig. 4 Comparison of total reflection spectra of silicon wafer, sparse SiNWs and dense SiNWs; inset images show the photos of sparse SiNWs and dense SiNWs.



(c)

Sample	J_{sc} (mA/cm²)	V_{oc} (V)	FF (%)	PCE (%)	Filling ratio (/mm²)
Sparse SiNWs	25.15	0.466	57.35	6.72	5.4×10^{7}
Dense SiNWs	9.80	0.380	34.65	1.29	1.8×10^{8}
Planar Si	5.85	0.466	19.53	0.53	—

Fig. 5 (a) Schematic diagram of the SiNW/PEDOT:PSS heterojunction solar cells; (b) light J–V curves, (c) table of performance parameters and (d) external quantum efficiency for tapered SiNWs/PEDOT:PSS hybrid solar cells with different nanowire filling ratios and for planar Si/PEDOT:PSS hybrid solar cells.

photovoltaic parameters including the short circuit current density (J_{sc}), open circuit voltage (V_{oc}), fill factor (FF) and power conversion efficiency (PCE) are given in the table (Fig. 5(c)). The PCE of the planar Si/PEDOT:PSS solar cells is 0.53%. Similar processing was used for the planar Si/PEDOT:PSS and SiNW/PEDOT:PSS cells, and the low efficiency of the planar cell may be attributable to the large surface reflection loss on the planar silicon wafer. For the sparse SiNWs solar cells, the highest PCE of 6.72% is obtained. Notably, the J_{sc} value for the sparse SiNW solar cells (25.15 mA cm^{-2}) is similar to that of previously reported SiNW/PEDOT:PSS cells employing nanowires fabricated by alternative techniques,[18,26–28] and exceeds that of the dense SiNW sample (9.8 mA cm^{-2}) by a factor of 2.56, despite the better anti-reflective properties of the dense tapered SiNWs. The increased J_{sc} is attributed to more effective filling of PEDOT:PSS into the sparse SiNWs *versus* the dense SiNWs, as was reported previously for short *versus* long nanowires.[18,19,29] Moreover, the external quantum efficiency (EQE) of these SiNWs solar cells was measured using a solar cell IPCE/QE measurement system. As we can see from Fig. 5(d), the EQE value of the sparse SiNWs is higher than that of the dense SiNWs in the wavelength range of 300–1100 nm, implying that the photogenerated carrier recombination in the sparse SiNWs is relatively weaker compared to the dense SiNWs.

These results indicate that the ability to control the filling ratio of tapered SiNWs demonstrated here is required to achieve a balance in the reduced reflection, the polymer infiltration and the carrier recombination, and hence to optimize the photovoltaic performance of the solar cells. Further enhancement in the PCE of these devices may result from optimizing the structural parameters of the tapered SiNWs, improving the contact between the SiNWs and PEDOT:PSS, increasing the conductivity of PEDOT:PSS, and so on.

Conclusions

In summary, we have reported a simple approach for fabricating tapered SiNW arrays with tunable filling ratios. A silver network catalyst with controllable porosity is sputtered onto silicon and a one-step wet etch is performed in a HF/H_2O_2 solution to produce tapered SiNWs. This method has the advantages of low cost, simple operational procedures, and no templates. By varying the patterns of the silver network, both dense (5.48×10^8 mm^{-2}) and sparse (1.57×10^8 mm^{-2}) SiNW arrays with the same thickness of 400 nm were produced in this work. The dense SiNWs showed the lowest average reflectance of 1.6% for wavelengths ranging from 300 to 1000 nm, whereas the sparse SiNWs performed better in preliminary SiNW/PEDOT:PSS heterojunction solar cells. A J_{sc} of 25.15 mA cm^{-2} and PCE of 6.72% were measured and attributed to the effective filling of PEDOT:PSS into the sparse SiNW arrays. The ability to both tapered SiNWs and tune their density using the simple technique presented in this work is relevant to the fabrication and optimization of low-cost optoelectronic devices in many fields.

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